CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a contact in a pixel sensor cell, comprising:

depositing a passivation layer over a substrate having pixel components;

forming a slot in the passivation layer in an area over a charge collection region of said pixel sensor cell;

implanting a dopant at an angle relative to sidewalls of the slot through said slot into said charge collection region; and

forming a contact within said slot.

2. The method of claim 1, wherein said slot has an oblong shape.

3. The method of claim 1, wherein said slot has an elliptical shape.

4. The method of claim 1, wherein said slot has an aspect ratio having a range of about 10:1 to 5:1.

5. The method of claim 1, wherein said dopant is implanted at an angle of about 20° relative to the sidewalls.

6. The method of claim 1, wherein said charge collection region is a floating diffusion region.

7. The method of claim 1, wherein said slot is etched in an insulator layer.

8. The method of claim 1, wherein said dopant is implanted at about 35 KeV.

9. The method of claim 1, wherein said dopant is implanted at an implant depth of about 300 Å to about 400 Å.

10. The method of claim 1 wherein said dopant is phosphorous.

11. A method of forming a contact in a pixel sensor cell comprising:

depositing a passivation layer over a substrate having pixel components;

forming a blocking layer extending over a portion of a charge collection region of said pixel sensor cell;

etching a slot into the passivation layer over said charge collection region, wherein said slot extends to contact said charge collection region over portions not covered by said blocking layer;

implanting a dopant at an angle relative to sidewalls of the slot through said slot into said charge collection region; and

forming a contact within said slot.

12. The method of claim 11, wherein said blocking layer includes at least one of polysilicon and silicon nitride.

13. The method of claim 11, wherein said slot has an oblong shape.

14. The method of claim 11, wherein said slot has an elliptical shape.

15. The method of claim 11, wherein said slot has an aspect ratio having a range of about 10:1 to 5:1.

16. The method of claim 11, wherein said dopant is implanted at an angle of about 20° relative to the sidewalls.

17. The method of claim 11, wherein said charge collection region is a floating diffusion region.

18. The method of claim 11, wherein said slot is etched in an insulator layer.

19. The method of claim 11, wherein said dopant is implanted at about 35 KeV.

20. The method of claim 11, wherein said dopant is implanted at an implant depth of about 300 Å to about 400 Å.

21. The method of claim 11, wherein said dopant is phosphorous.

22. A pixel sensor cell comprising:

a first slot formed in a passivation layer over a charge collection region;

a dopant implant region formed in said charge collection region underneath said first slot; and

a first contact formed through said first slot, wherein said first contact has a footprint larger than other contacts formed in said pixel sensor cell.

23. The pixel sensor cell of claim 22, wherein said first slot has a footprint having an oblong shape.

24. The pixel sensor cell of claim 22, wherein said first slot has a footprint having an elliptical shape.

25. The pixel sensor cell of claim 22, wherein said charge collection region is a floating diffusion region.

26. The pixel sensor cell of claim 22, wherein said first slot is etched in an insulator layer.

27. The pixel sensor cell of claim 22, further comprising a layer of a blocking material, wherein said blocking material extends from an adjacent gate stack and thereby decreases a size of said footprint over said charge collection region.

28. An imaging device, comprising:

an array of pixel sensor cells formed in said doped layer, wherein each pixel sensor cell comprises:

a first slot formed in a passivation layer and over a charge collection region, a dopant implant region formed in said charge collection region underneath said first slot and a first contact formed through said first slot, wherein said first contact has a footprint larger than other contacts formed in said pixel sensor cell; and

signal processing circuitry formed in said substrate and electrically connected to the array for receiving and processing signals representing an image output by the array and for providing output data representing said image.

29. The imaging device of claim 28, wherein said first slot has a footprint having an oblong shape.

30. The imaging device of claim 28, wherein said first slot has a footprint having an elliptical shape.

31. The imaging device of claim 28, wherein said charge collection region is a floating diffusion region.

32. The imaging device of claim 28, wherein said first slot is etched in an insulator layer.

33. The imaging device of claim 28, further comprising a layer of a blocking material, wherein said blocking material extends from an adjacent

gate stack and thereby decreases a size of said footprint over said charge collection region.

34. A processing system comprising:

a processor; and

an imaging device coupled to said processor, said imaging device having at least one pixel sensor cell comprising:

a first slot formed in a passivation layer of said pixel sensor cell and over a charge collection region, a dopant implant region formed in said charge collection region underneath said first slot and a first contact formed through said first slot, wherein said first contact has a footprint larger than other contacts formed in said pixel sensor cell; and

a readout circuit comprising at least an output transistor formed on said substrate.

35. The system of claim 34, wherein said first slot has a footprint having an oblong shape.

36. The system of claim 34, wherein said first slot has a footprint having an elliptical shape.

37. The system of claim 34, wherein said first slot is etched in an insulator layer.

38. The system of claim 34, further comprising a layer of a blocking material, wherein said blocking material extends from an adjacent gate stack and thereby decreases a size of said footprint over said charge collection region.